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Alignment Technology for Backside Integration

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ABSTRACT

This paper presents a backside-to-frontside alignment technique for the backside processing of Si wafers. Integrated MEMS components like BiCMOS-embedded RF-MEMS switches require accurate (1-2µm) alignment. We demonstrate an alignment technique providing overlay values of less than 500 nm by using a backside alignment layer. The approach is enabled by a new non-contact wafer pre-alignment system of the Nikon Scanner S207D allowing precise loading (<5µm) of the wafer onto the exposure stage. Before starting the back-side MEMS process, the misalignment between frontside devices and backside alignment layer has to be measured. The alignment errors are applied as lithography overlay corrections to the backside MEMS process. For the specific application of deep Si etching (Bosch process), moreover, one has to consider the etch profile angle deviation across the wafer (tilting), which turned out in our experiments to amount up to 8 µm. During initial experiments with a Nikon i-line stepper NSR-2205 i-11D the overlay has been corrected by the stepper offset parameters. These parameters have been obtained by summing up both the wafer and intra-field scaling errors caused by deep Si etching and backside-to-frontside alignment errors. Misalignments and tilting errors were all measured with a MueTec MT 3000 IR optical metrology system using overlay marks.

The developed alignment technique is applied to BiCMOS-embedded MEMS devices, i.e. mm-wave RF switches and a viscosity sensor chip based on the IHP's high-speed SiGe technology. It turned out to be very promising for backside processed MEMS components with critical alignment requirements.

Key Words: MEMS, backside-to-frontside alignment, backside-to-frontside overlay, Bosch process, deep-silicon dry-etch, backside lithography, IR microscopy

1. INTRDUCTION

The usage of the back site of the wafer requires accurate backside-to-frontside alignment. That is interesting e.g. for RF-MEMS switches and biosensors or high-Q passives like antennas and coils suitable for the 10-100 GHz frequency range all require large Si-free cavities or low-ε regions beneath them for lowest parasitics /1, 2/. In these cases, silicon from the substrate has to be removed by applying a deep-silicon dry-etch technique as, for instance, the Bosch process /3/ from the wafer backside. For example, RF-MEMS switches are considered as key components to fulfill the beam steering and phase array antenna requirements of mm-wave applications /1, 2/ thereby enabling imaging systems to work in the 122GHz ISM band. For such high frequency applications, a monolithic, embedded integration of the switch with a high-performance CMOS or BiCMOS platform would be superior to heterogeneous integration with the basic IC process, because it provides the shortest connections and lowest misalignment between switch and circuitry resulting in the low parasitics. In the same way high-Q on-chip inductors, and antennas also provide short connection paths and low-loss on-chip interconnection with low parasitic /1, 2/ and small (1-2µm) misalignment /1/. In addition, backside etching is of importance for integration of sensors in the BiCMOS BEOL process like the IHP glucose sensor, which is fabricated as a MEMS viscosimeter /4, 5/.

A stringent necessity for these backside-integrated devices is a correct backside-to-frontside wafer alignment with overlay values of less than 1-2µm, since otherwise RF-MEMS with asymmetric mechanical structures and undefined behavior would result /1/. Due to the shrinking process of ICs for mm-wave applications even smaller passive components with shortest transmission lines require such overlay values to minimize losses or parasitics.

State-of-the-art backside deep-silicon etching techniques like the Bosch process cause a radial misalignment between frontside and backside of the wafer /6, 7/, which is intrinsically coupled to the plasma etching process itself and is known as tilting error. The stringent overlay constraints as mentioned above cannot be achieved without any correction of these process related position errors. Recent backside lithography tools make use of special alignments systems, compare, for instance, the ULTRATECH wafer stepper /8/, the ASML wafer scanner /9, 10/, or the SUSS MicroTec Lithography and EV Group mask aligners.

Here, we propose to use conventional lithography tools with a precise ($3\sigma X$, $3\sigma Y$, $3\sigma\theta < 5\ \mu m$) pre-alignment technique as it can be performed with the Nikon Scanner S207D. After structuring the backside alignment layer with the S207D, an i-line exposure is done comprising the overlay correction of the alignment layer (OVL_{Align}) and the etching position error of the backside layer (ETCH ERROR). The backside exposure offsets, wafer translation, rotation and expansion have been calculated from raw data produced by a MueTec MT 3000 IR microscope /11/.

2. EXPERIMENTAL

Wafer Processing

The backside-to-frontside alignment scenario together with the MEMS backside integration strategy is illustrated in Figure 1. Additional overlay marks (Fig. 1) have been included along with the MEMS preparation on the frontside of the wafer (SEMI standard 8-inch). Overlay marks were prepared from a standard metal layer stack (Ti/TiN/AlCu/TiN) in order to achieve a high IR contrast. The wafer was rotated around the y axis for all backside exposures. The backside alignment layer lithography was carried out by the new pre-alignment system of Nikon Scanner S207 with a chemical amplified positive resist UV5 (DOW). The exposed backside alignment layer contains alignment and backside overlay marks (Fig. 1). This pattern has been etched 100nm in the silicon after checking the overlay values from the pre-alignment.

Alignment corrections for the subsequent i-line stepper process were calculated from a six parameter model /12/. These misalignment errors affected the lithography positions offsets corrections for the backside MEMS lithography layer of each wafer.

The silicon backside etching process has been performed through the full wafer using the well known Bosch process and a standard deep silicon etcher (Tegal 200). A 4500 nm thick PECVD oxide layer was applied as hard mask. The deep Si etching leads to position errors varying across the wafer^. These lead to further corrections by applying lithography scaling offsets.

Prealignment

The Nikon contactless pre-alignment system (Fig. 2) enables a precise loading of the wafer on the wafer stage. For this purpose, a notch orientation is carried out firstly, while the final fine alignment is performed just before the wafer is loaded onto the wafer chuck. This is done by moving the wafer together with the pre-alignment arm using the CCD cameras for the identification of wafer edge and notch position at three points and calculates the center position as well as the wafer rotation for the final corrections. The loading position reproducibility exhibits a 3σ error of less than 5µm for x, y and y_1-y_2 coordinates.

Matching the centers of pre-alignment loading position and wafer stage is necessary, because the position error is doubled by rotating the wafer along its y axis for switching from frontside to backside processing.

Overlay Measurement

Measurements of the overlay were performed at back-to-front overlay marks with an infrared microscope MT 3000 IR for a coarse adjustment. The MT 3000 IR is a fully automated measurement and inspection tool using optimized objectives in the spectral range between 1050 and 1550 nm. The tool integrated software is able to determine the backside-to-frontside overlay and may also perform die-to-die inspection and review tasks like sealing inspection /11/. Layouts of different size and shape were included in the test mask to check for the best overlay target for the IR microscope MT 3000 IR. An example for frame-in-frame marks using IR transmitted light is given in Figure 3.

Figure 4 shows the schematic of the position error measurement for backside deep Si etching and the respective image of overlay marks. The final results were corrected by Tool Induced Shift (TIS) using the measurements with 180° rotated orientation.

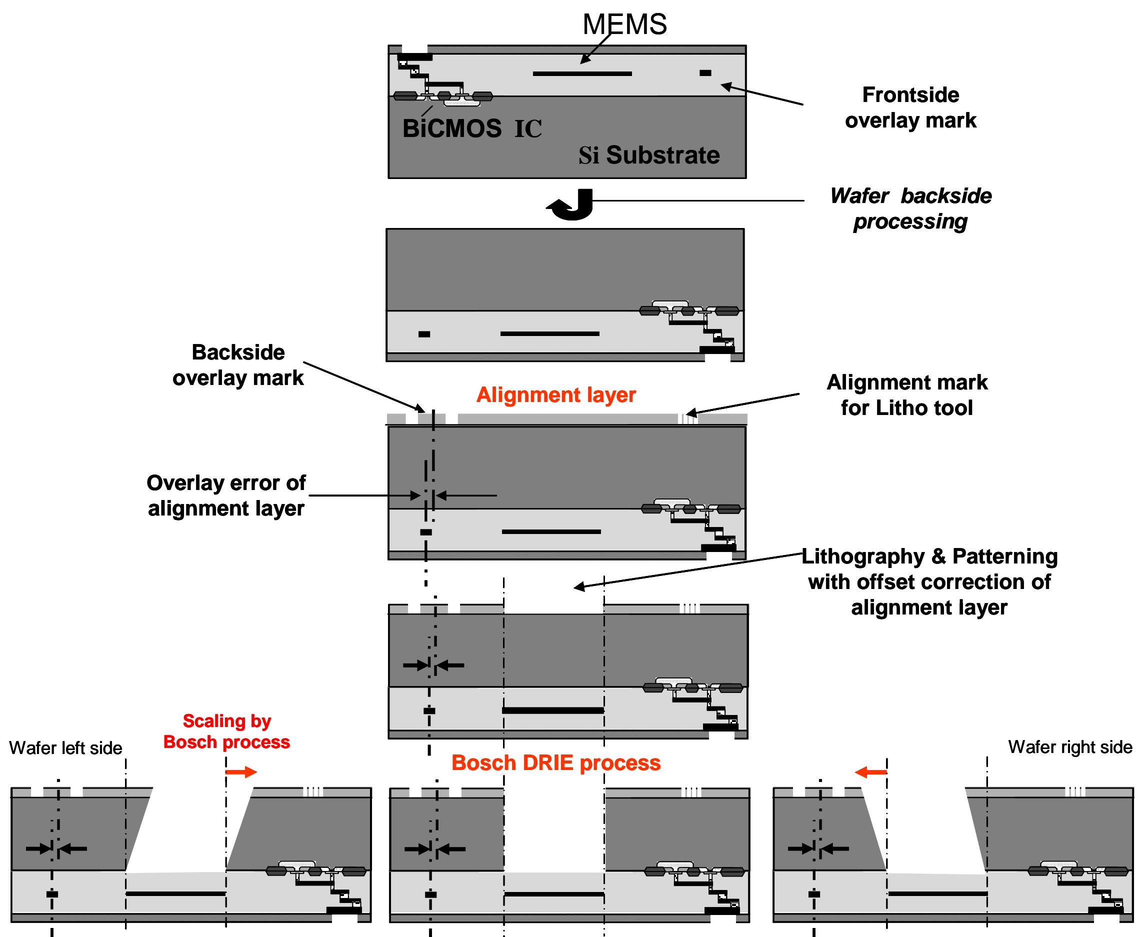


Fig. 1: Concept of backside processed MEMS integration and backside-to-frontside alignment scenario.

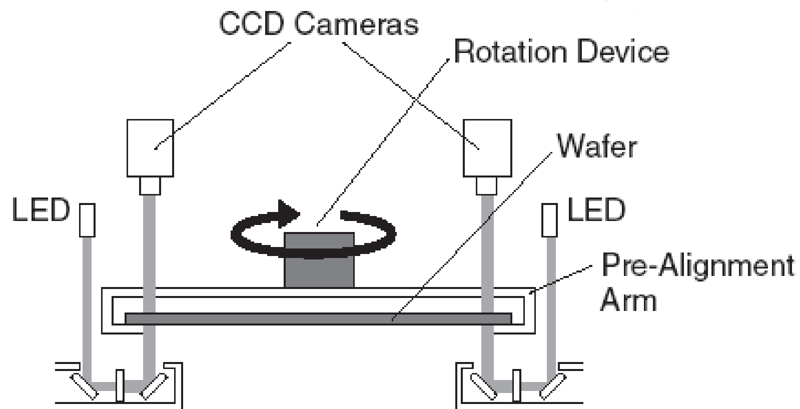
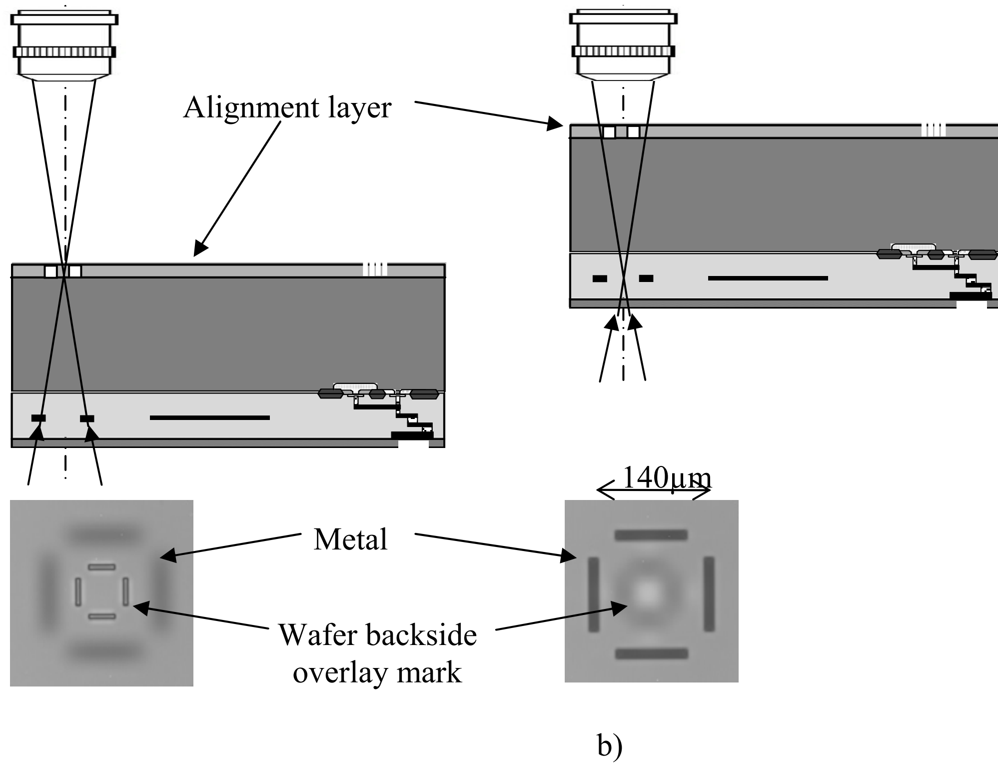
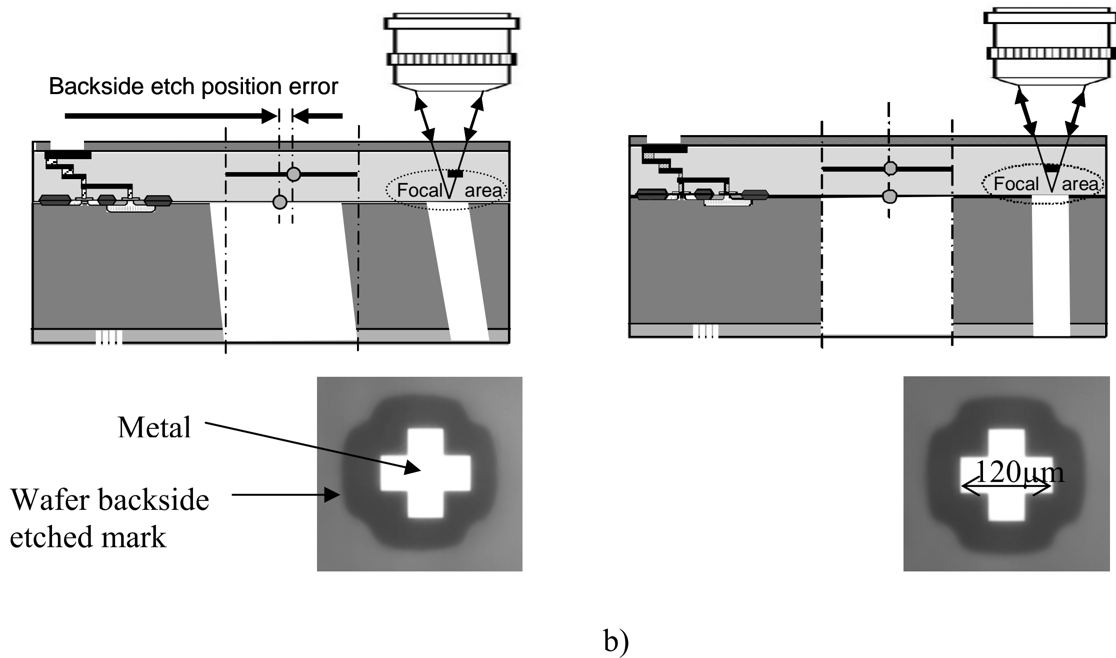


Fig. 2: Schematics for Nikon non-contact pre-alignment system unit



a) b)

Fig. 3: Backside metal overlay mark (a) and frontside overlay mark (b) for top and backside focusing of the transmitted IR-light (20x objective).



a) b)

Fig. 4: Schematic of backside position error (ETCH ERROR) measurement and overlay pattern in the case of a) wafer edge (≈8µm Position error) and b) wafer center (<0.5µm overlay error) using reflected light.

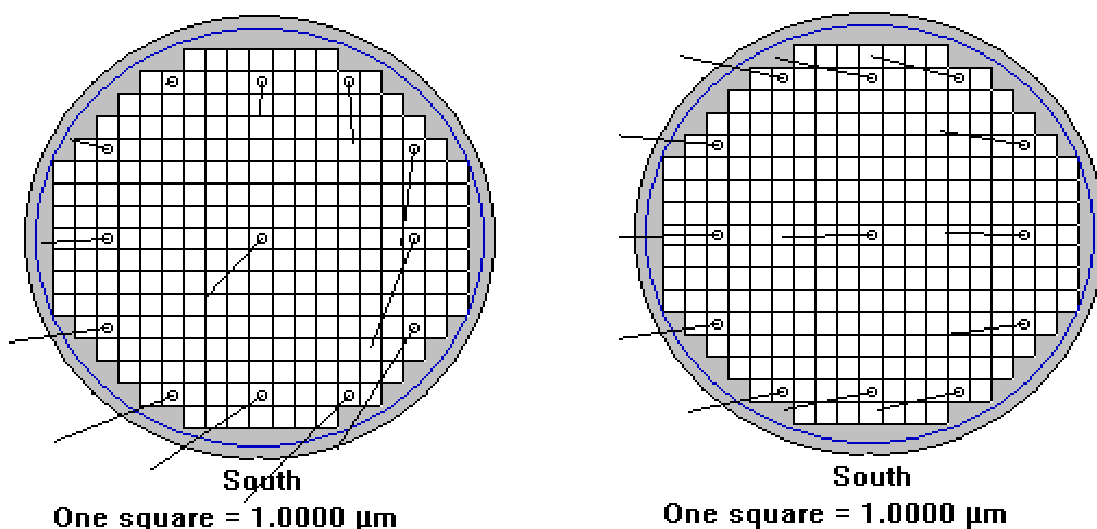


Fig. 5: Vector displacement map of the overlay errors Dx_{Align} and Dy_{Align} between backside alignment layer and frontside metal layer of wafer 3(left) and 4(right).

Table 1: Backside-to-frontside overlay errors determined from the displacement error between the backside alignment layer and the frontside metal layer

Wafer	After prealignment					
	x mean µm	$3\sigma_x$ µm	Overlay x µm	y mean µm	$3\sigma_y$ µm	Overlay y µm
1	0.69	1.25	**1.94**	-1.83	2.17	**3.99**
2	-3.35	4.40	**7.74**	0.12	4.35	**4.46**
3	-2.65	6.09	**8.74**	-2.52	6.04	**8.55**
4	-4.27	1.28	**5.55**	0.03	2.17	**2.20**
5	-2.67	1.26	**3.93**	-1.93	2.32	**4.24**
6	-2.45	2.97	**5.43**	-0.47	3.42	**3.89**
Mean	-2.45	2.87	**5.55**	-1.10	3.41	**4.56**

Table 2: Lithography offsets corrections for the first backsides integrated MEMS layer analyzed using the six parameter model based on Table 1

Wafer	Lithography Offsets					
	$XTran_{Align}$ µm	$YTran_{Align}$ µm	$XScal_{Align}$ ppm	$YScal_{Align}$ ppm	$Ortho_{Align}$ µrad	Rot_{Align} µrad
1	-0.69	-1.83	8.21	13.10	1.24	-0.43
2	-3.32	0.13	8.17	13.70	0.88	24.60
3	-2.67	-2.55	8.55	13.40	1.31	-37.20
4	-4.26	0.02	8.00	13.00	1.07	1.38
5	-2.67	-1.94	8.29	14.00	0.69	-0.19
6	-2.46	-0.49	8.18	13.20	1.04	-17.40

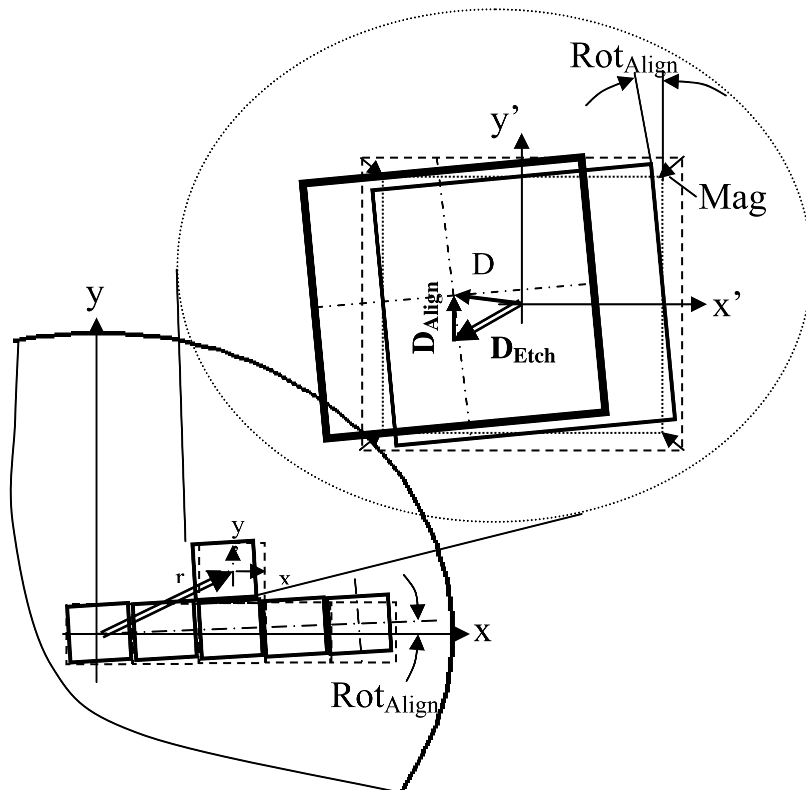


Fig. 6: Schematic of offsets for the backside layer and etch tilt correction

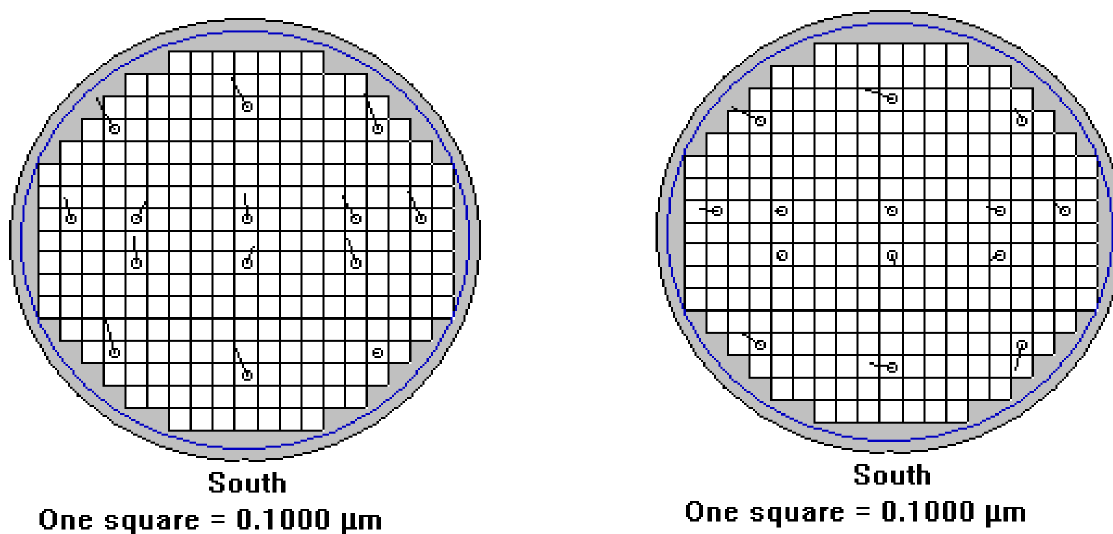


Fig. 7: Vector displacement map of backside-to-frontside overlay errors after offsets corrections for the first backsides integrated MEMS layer of wafer 3(left) and 4(right).

Table 3: Results of backside-to-frontside overlay errors after offsets corrections for backside integrated MEMS layer

Wafer	After correction					
	x mean µm	$3\sigma_x$ µm	Overlay x µm	y mean µm	$3\sigma_y$ µm	Overlay y µm
1	-0.07	0.15	**0.22**	0.05	0.18	**0.23**
2	-0.10	0.12	**0.22**	-0.03	0.13	**0.17**
3	-0.04	0.12	**0.16**	0.12	0.12	**0.23**
4	-0.07	0.13	**0.20**	0.01	0.14	**0.15**
5	-0.06	0.38	**0.44**	-0.10	0.29	**0.39**
6	-0.04	0.29	**0.33**	0.05	0.17	**0.22**
Mean	-0.06	0.20	**0.26**	0.01	0.17	**0.23**

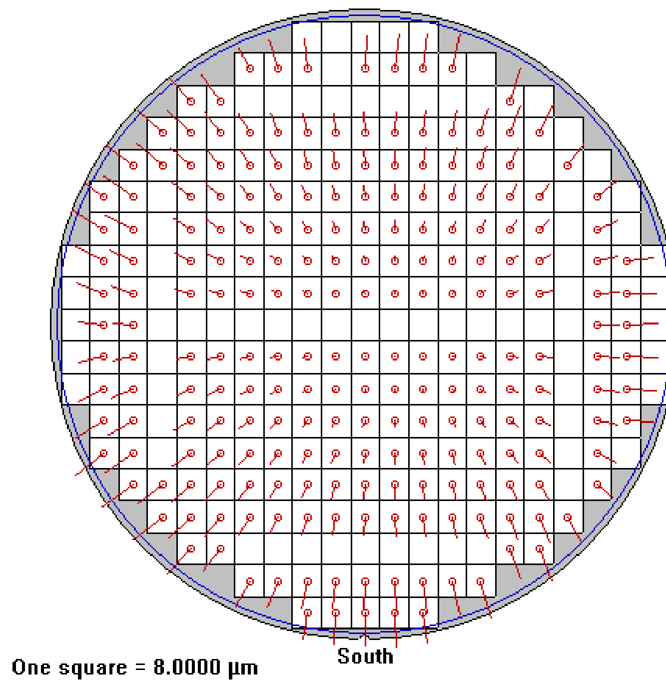


Fig. 8: Vector displacement map of the ETCH ERROR after the Bosch process as measured for wafer 5.

3. RESULTS AND DISCUSSION

Results of the overlay measurement as performed for the backside alignment layer exposed by using the Nikon pre-aliignment technique are shown in Figure 5 and Table 1. The measured overlay errors in units of mean+3σ are found to be between 2μm and 9μm. The calculated backside exposure offsets are given in Table 2.
The exposure job for MEMS layer includes the map correction $D(x, y)$ considering the OVL_{Align} and the ETCH ERROR.

$$D(x, y) = D_{Align}(x, y) + D_{Etch}(x, y) \quad (1)$$

Here, x and y represent the wafer coordinate frame and the offset for the backside exposure can be calculated from the overlay measurement OVL_{Align} and a six parameter model /12/.

$$Dx_{Align} = XTrans_{Align} + XScal_{Align} * x - XRot_{Align} * y \quad (2)$$
$$Dy_{Align} = YTrans_{Align} + YScal_{Align} * y + YRot_{Align} * x$$

The following equations describe the special Nikon i-line map offset.

$$Dx_{Align} = XTrans_{Align} + XScal_{Align} * x - (Rot_{Align} + Ortho_{Align}) * y \quad (3)$$
$$Dy_{Align} = YTrans_{Align} + YScal_{Align} * y + Rot_{Align} * x$$

The set of parameters including wafer translation ($XTrans_{Align}$, $YTrans_{Align}$), wafer scaling ($XScal_{Align}$, $YScal_{Align}$), wafer rotation ($Rot_{Align}= YRot_{Align}$) and wafer orthogonality ($Ortho_{Align}= XRot_{Align} - YRot_{Align}$) was determined by comparing overlay measurements from the backside alignment layer with those from the frontside layer.
The ETCH ERROR, which was determined by measuring the position error after the Bosch process, is generally a scaling error caused by the etch tilt across the wafer

$$Dx_{Etch} = XScal_{Etch} * x \quad (4)$$
$$Dy_{Etch} = YScal_{Etch} * y$$

The final scaling offset is the sum of the wafer scaling of the alignment layer ($XScal_{Align}$, $YScal_{Align}$) and the etch scaling ($Xscal_{Etch}$, $Yscal_{Etch}$).

$$Dx = XTrans_{Align} + (XScal_{Align} + XScal_{Etch}) * x - (Rot_{Align} + Ortho_{Align}) * y \quad (5)$$
$$Dy = YTrans_{Align} + (YScal_{Align} + YScal_{Etch}) * y + Rot_{Align} * x$$

Assuming a radial symmetric ETCH ERROR ($Scal_{Etch}=XScal_{Etch}=YScal_{Etch}$) leads to

$$Dx = XTrans_{Align} + (XScal_{Align} + Scal_{Etch}) * x - (Rot_{Align} + Ortho_{Align}) * y \quad (6)$$
$$Dy = YTrans_{Align} + (YScal_{Align} + Scal_{Etch}) * y + Rot_{Align} * x$$

A geometrical scheme is shown in Fig. 6.
The intrafield correction (Dx', Dy') was done by shot magnification (Mag) and shot rotation. In our case, the shot rotation is defined by the wafer rotation.

$$Dx' = Mag * x' - Rot_{Align} * y' \quad (7)$$
$$Dy' = Mag * y' + Rot_{Align} * x'$$

Here, x' and y' represent the field coordinate frame. A numerical value for $Scal_{Etch}$ between -80 and -90 ppm was measured after applying the deep Si etch through the full wafer of 750 μm thickness, see Fig.10. These corrections are

beyond the lens magnification offset limits. Due to the limited intrafield magnification offset of the Nikon stepper, the minimum magnification correction ($Mag = Mag_{min}$ = -30ppm) was applied. The error caused by this approximation may result in absolute deviations of less than 0.7µm for maximum field size. This value might also be used as a magnification correction of mask layout for an improved correction.

Moreover, it can be seen from Fig. 7 and Table 3 that the absolute value of OVL_{Align} could be reduced below 500 nm, which demonstrates the technological potential of the backside exposure method.

The ETCH ERROR and etch tilt are shown in Figures 8, 9, and 10, respectively. The data analysis demonstrate an asymmetry of the ETCH ERROR. The $YScal_{Etch}$ is about 7 ppm higher than the $XScal_{Etch}$ for the test pattern and IHP MEMS device respectively.

Fig 9 shows the tilts as a function of the radial positions over the wafer. The tilt angle varies form nearly 0° at the wafer center to 0.6° at the wafer edge. The latter value exceeds the best tilt angle, which was specified to amount to 0.2° by the tool supplier /7/. The tilting is probably caused by ions travelling to the wafer surface along non-perpendicular trajectories. There are a couple of reasons for this phenomenon to occur /7/. One reason can be that the sheath generated between plasma and wafer is not perfectly parallel to the wafer surface, which may particularly appear close to the wafer edge because of the chuck design. Therefore, the ions accelerated by passing the sheath in this region are deflected from the ideal vertical direction. Furthermore, a high etch rate is necessary for etching through the full wafer in reliable process time implying that gas flows, source and bias power should be high. The latter parameters, however, affect the sheath thickness and may distort sheath uniformity, which may induce ion steering and an oblique etch process. In addition, also a wafer layout with non-uniform distribution of open area can be a reason for tilting, if the allocation is associated with the occurrence of local charges. Finally, Figure 9 and 10 reveal an obvious non-linearity of the tilting and ETCH ERROR that is particularly pronounced at the wafer border. Both effects (asymmetry and the non-linearity) were not considered in the offset correction so far. However, their inclusion into the correction formalism has great potential for further improving the backside-to-frontside alignment performance. Future work will have to consider these effects in more detail for further reducing the angle of deviation across the wafer.

Figure 10 demonstrates the successful correction of the alignment procedure. The backside-to-frontside overlay deviation can be reduced to values of less than 2.0µm in terms of mean +3σ. The offset correction was carried out using a $Scal_{Etch}$ of -77ppm (Fig. 10). It can be seen that the $Scal_{Etch}$ values differ by about 5ppm when comparing the MEMS device layer (about -80ppm according to ETCH ERROR) and the test pattern layer (about -85ppm). This observation might be understood from dependence of $Scal_{Etch}$ on layout or dimension.

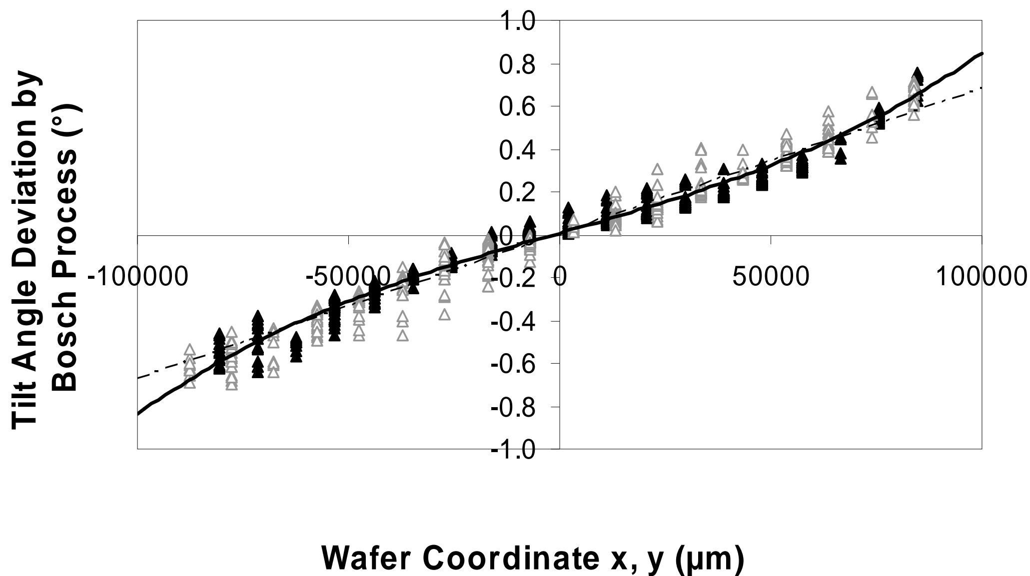


Fig. 9: Tilt angle deviation across a 200mm wafer derived from the position measurements after the Bosch deep Si etch process (wafer 5 and 6 with test pattern, $angle_x$(▲), $angle_y$(△)).

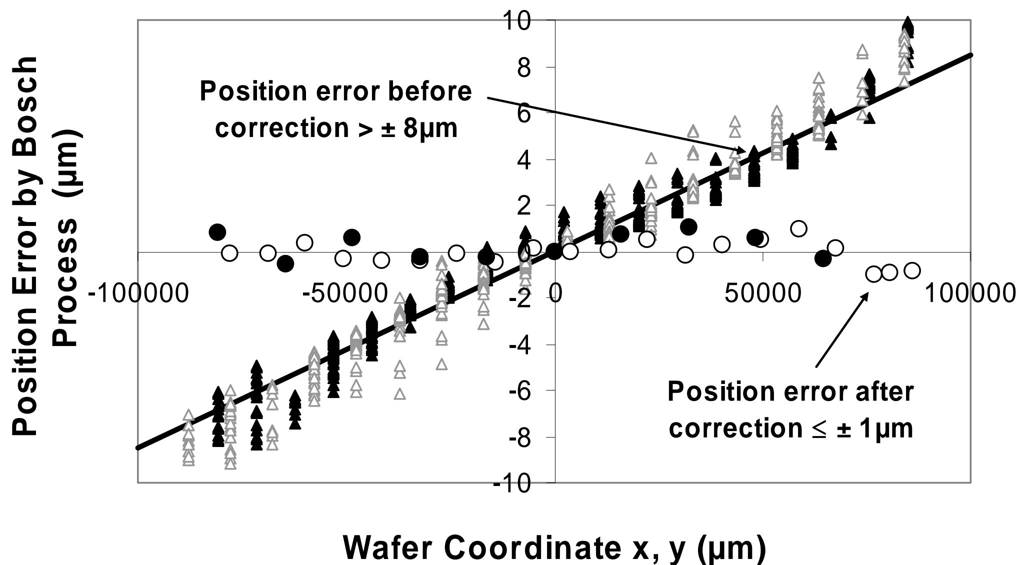


Fig. 10: Position error after deep-silicon dry-etch technique (BOSCH-process) without correction and after correction (wafer 5 and 6 with test pattern, ETCH $ERROR_x$(▲), ETCH $ERROR_y$(△) and MEMS final overlay error x(●), **y**(○)).

4. CONCLUSION

A precise pre-alignment in combination with a backside alignment layer has been shown to enable a BiCMOS-embedded MEMS integration. The results presented in this work demonstrate that the backside-to-frontside alignment is a suitable method for achieving an alignment accuracy of better than 500 nm. Also the position error caused by removing silicon under the MEMS by deep-silicon dry-etching can be corrected by using this method with an accuracy of better than 2 µm in mean +3σ. It has to be emphasized that an accurate and flexible infrared microscope is inevitable for achieving this alignment accuracy. Further improvements appear possible, when the asymmetry and non-linearity of the backside etching process would be included into the correction formalism.
The fact that no particular backside lithography tool is required can be considered as a big advantage of the presented approach. The requirement of an additional alignment layer, however, which is tolerable only for research and pilot production, might be regarded as disadvantage.
To summarize, the backside-to-frontside alignment technique has successfully been applied to BiCMOS-embedded MEMS devices based on IHP's high-speed SiGe technology like mm-wave RF switches and a viscosity sensor. The developed technique appears very promising for MEMS components in general that require a precise backside-to frontside alignment.

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